Questions for self assessment

Module 7--Lecture 1

1. What is the role of testing in VLSI design flow?
2. What are the basic differences between VLSI testing and "classical" testing philosophy?
3. What are the different types of tests that can be performed on a 2 input NAND gate

Module 7--Lecture 2

1. What is functional testing? Why functional testing is difficult to be performed on a complex circuit?

2. What is structural testing and how it can address the issues of functional testing?

3. Why some additional circuitry called "design for testability" is required in structural testing?

4. What are the pros and cons of structural testing compared to functional testing?

5. What is fault model? What are the characteristics of a good fault model? Why stuck at fault model is widely accepted?

Module 7--Lecture 3

1. What is fault equivalence and fault dominance?

2. How does fault equivalence and fault dominance help in lowering the complexity of testing?

3. Among two input AND, OR, NAND, NOR, NOT, XOR, XNOR gates, where fault collapsing is not possible using equivalence?

4. A circuit has *n* inputs and *n* outputs. It is implemented only using AND, OR and NOT gates. Further, there are no fan-out branches. What is the number of s-a faults that remain after fault collapsing?

5. What is the problem, from the context of fault collapsing (using equivalence or dominance), if a circuit has lots of fanouts?